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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/751,129	12/29/2000	Russell E. Henning	INTL-0501-US (P10387)	9172

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TROP PRUNER & HU, PC
8554 KATY FREEWAY
SUITE 100
HOUSTON, TX 77024

EXAMINER	
RAO, ANAND SHASHIKANT	

ART UNIT	PAPER NUMBER
2613	

DATE MAILED: 08/09/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/751,129	HENNING, RUSSELL E.	
	Examiner	Art Unit	
	Andy S. Rao	2613	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on *10 May 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-28, 30-33* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-28, 30-33* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

1. Applicant's arguments filed in Paper 9 on 5/10/04 with respect to amended claims 1-28 and 30-33 have been fully considered but they are not persuasive.

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1-2, 6-8, 19-23, 25-28, 30-32 (amended) remain rejected under 35 U.S.C. 103(a) as being unpatentable over Sun et al., (hereinafter referred to as "Sun") in view of Shiomoto.

4. Claims 3-5, 9, and 24 (amended) remain rejected under 35 U.S.C. 103(a) as being unpatentable over Sun et al., (hereinafter referred to as "Sun") in view of Shiomoto as applied to claims 1 and 22 above, and further in view of Webb.

5. Claims 10-18 (amended) remain rejected under 35 U.S.C. 103(a) as being unpatentable over Sun et al., (hereinafter referred to as "Sun") in view of Shiomoto and Webb.

6. The Applicants present one argument contending the Examiner's rejection of claims 1-2, 6-8, 19-23, 25-28, 30-32 (previously presented) under 35 U.S.C. 103(a) as being unpatentable over Sun et al., (hereinafter referred to as "Sun") in view of Shiomoto, the rejection of claim s 3-5, 9, and 24 (previously presented) under 35 U.S.C. 103(a) as being unpatentable over Sun et al., (hereinafter referred to as "Sun") in view of Shiomoto as applied to claims 1 and 22 above, and further in view of Webb, and rejection of claims 10-18 (previously presented) under 35 U.S.C. 103(a) as being unpatentable over Sun et al., (hereinafter referred to as "Sun") in view of

Shiomoto and Webb, as was set forth in the previous Office Action of Paper 8 mailed on 4/07/04, wherein the presented arguments now attempt establish patentability over the previously used references on the basis of the added limitations. However, after careful consideration of the arguments presented, the Examiner must respectfully disagree, and maintain the grounds for rejection from the references as sufficient to meet the newly added limitations for the reasons that follow below.

Firstly, the Applicants argue that Shiomoto fails to disclose "a second error resilience technique which replaces a bit pattern for the second type of frame with a shorter length..." as in the claims (Paper 9: page 7, lines 1-23). The Examiner respectfully disagrees. It is noted that Shiomoto discloses coding correcting parity bits of added to the second frame of a length that is short than the first length (Shiomoto: column 4, lines 25-40). Accordingly, the Examiner maintain that Shiomoto would met this limitation as well.

A detailed Office Action addressing the newly added limitation follows below.

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. Claims 1-2, 6-8, 19-23, 25-28, 30-33 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sun et al., (hereinafter referred to as "Sun") in view of Shiomoto.

Sun discloses an apparatus comprising: a first block to process a first type of frame in a video bitstream (Sun: column 7, lines 50-65; column 9, lines 45-56); and a second block to process a second type of frame in the video bitstream (Sun: column 10, lines 5-10 & 40-67), as in claim 1. However, Sun fails to disclose using first and second error resiliency techniques with the respective first and second blocks. Shiomoto discloses an error concealment apparatus with differing error resiliency techniques based differing code strings (Shiomoto: column 4, lines 10-60) wherein the second error resilience technique replaces a bit pattern from the second type of frame with a shorter bit pattern (Shiomoto: column 4, lines 30-45) in order to reinforce error-correcting abilities (Shiomoto: column 2, lines 1-6). Accordingly, given this teaching, it would have been obvious for one of ordinary skill in the art to incorporate Shiomoto's differing error concealment techniques for improved error resiliency into the Sun apparatus in order to reinforce error-correcting abilities. The Sun apparatus, now incorporating Shiomoto's differing error resiliency techniques for the first and second frames, has all of the features of claim 1.

Regarding claim 2, the Sun apparatus, now incorporating Shiomoto's differing error resiliency techniques for first and second frames, has the first block also processing a third type of frame (Sun: column 10,lines 5-10), as in the claim.

Regarding claim 6, the Sun apparatus, now incorporating Shiomoto's differing error resiliency techniques for the first and second frames, has the second block insert fewer error resilience bits in the video bitstream than the first block (Shiomoto: column 4, lines 40-50), as in the claim.

Regarding claims 7-8, the Sun apparatus, now incorporating Shiomoto's differing error resiliency techniques for the first and second frames, has third and fourth blocks for differing error concealment techniques (Sun: column 6, lines 23-50), as in the claims.

Sun discloses an apparatus comprising: a first block to process a first type of frame in a video bitstream (Sun: column 7, lines 50-65; column 9, lines 45-56); and a second block to process a second type of frame in the video bitstream (Sun: column 10, lines 5-10 & 40-67), as in claim 19. However, Sun fails to disclose using first and second error concealment techniques with the respective first and second blocks. Shiomoto discloses an error concealment apparatus with differing error resiliency techniques based differing code strings (Shiomoto: column 4, lines 10-60) wherein the second error resilience technique replaces a bit pattern from the second type of frame with a shorter bit pattern (Shiomoto: column 4, lines 30-45) in order to reinforce error-correcting abilities (Shiomoto: column 2, lines 1-6). Accordingly, given this teaching, it would have been obvious for one of ordinary skill in the art to incorporate Shiomoto's differing error concealment techniques for improved error resiliency into the Sun apparatus in order to reinforce error-correcting abilities. The Sun apparatus, now incorporating Shiomoto's differing error concealment techniques for the first and second frames, has all of the features of claim 19.

Regarding claim 20, the Sun apparatus, now incorporating Shiomoto's differing error concealment techniques for the first and second frames, has a variable length decoder block (Sun: column 9, lines 15-21), as in the claim.

Regarding claim 21, the Sun apparatus, now incorporating Shiomoto's differing error concealment techniques for the first and second frames, has the second error concealment technique comprising a block copy (Sun: column 12, lines 1-40), as in the claim.

Sun discloses a method comprising: receiving a video stream (Sun: column 7, lines 39-52); performing a first processing step a first type of frame in a video bitstream (Sun: column 7, lines 50-65; column 9, lines 45-56); performing a second processing step on a second type of frame in the video bitstream (Sun: column 10, lines 5-10 & 40-67), as in claim 22. However, Sun fails to disclose using first and second error resiliency techniques with the respective first and second blocks. Shiomoto discloses an error concealment apparatus with differing error resiliency techniques based differing techniques (Shiomoto: column 4, lines 10-60; column 8, lines 55-67) wherein the second error resilience technique replaces a bit pattern from the second type of frame with a shorter bit pattern (Shiomoto: column 4, lines 30-45) in order to reinforce error-correcting abilities (Shiomoto: column 2, lines 1-6). Accordingly, given this teaching, it would have been obvious for one of ordinary skill in the art to incorporate Shiomoto's differing error concealment techniques for improved error resiliency into the Sun method in order to reinforce error-correcting abilities. The Sun method, now incorporating Shiomoto's differing error resiliency techniques for the first and second frames, has all of the features of claim 22.

Regarding claim 23, the Sun method, now incorporating Shiomoto's differing error resiliency technique for first and second frames, performing error resiliency on an I frame (Sun: column 10, lines 25-30), as in the claim.

Regarding claim 25, the Sun method, now incorporating Shiomoto's differing error resiliency techniques for the first and second frames, has the second technique inserts fewer error resilience bits in the video bitstream than the first error resilience technique (Shiomoto: column 4, lines 40-50), as in the claim.

Regarding claim 26, the Sun method, now incorporating Shiomoto's differing error resiliency techniques for first and second frames, has the second technique insert fewer error resilience bits into the video bitstream than the first technique (Sun: column 10, lines 40-65), as in the claim.

Sun discloses an apparatus (Sun: figures 6-7) comprising: a first block to perform error concealment on an encoded video signal to provide an output signal (Sun: column 3, lines 10-20); a second block to determine at least one channel characteristic (Sun: column 12, lines 53-67; column 13, lines 1-13); and a third block to perform resilience on the output signal based on at least one channel characteristic and provide a modified video signal (Sun: column 10, lines 20-30), as in claim 27. However, Sun fails to disclose using first and second error resiliency techniques with the respective first and second blocks. Shiomoto discloses an error concealment apparatus with differing error resiliency techniques based differing code strings (Shiomoto: column 4, lines 10-60) wherein the second error resilience technique replaces a bit pattern from the second type of frame with a shorter bit pattern (Shiomoto: column 4, lines 30-45) in order to reinforce error-correcting abilities (Shiomoto: column 2, lines 1-6). Accordingly, given this teaching, it would have been obvious for one of ordinary skill in the art to incorporate Shiomoto's differing error concealment techniques for improved error resiliency into the Sun apparatus in order to reinforce error-correcting abilities. The Sun apparatus, now incorporating Shiomoto's differing error resiliency techniques for the first and second frames, has all of the features of claim 27.

Regarding claim 28, the Sun apparatus, now incorporating Shiomoto's differing error resiliency techniques for the first and second frames, discloses transmitting the modified signal to a storage device (Sun: column 12, lines 45-53), as in the claim.

Regarding claim 30, the Sun apparatus, now incorporating Shiomoto's differing error resiliency techniques for the first and second frames, that the first error concealment technique is different than the second technique (Sun: column 12, lines 1-40), as in the claim.

Regarding claims 31 and 33, the Sun apparatus, now incorporating Shiomoto's differing error resiliency techniques for the first and second frames, discloses that the first frames are I frames and the second frames are B frames (Shiomoto: column 8, lines 65-67; column 9, lines 1-10), as in the claims.

Regarding claim 32, the Sun apparatus, now incorporating Shiomoto's differing error resiliency techniques for the first and second frames, discloses that the third frames are I frames (Shiomoto: column 8, lines 65-67; column 9, lines 1-10), as in the claim.

9. Claims 3-5, 9, and 24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sun et al., (hereinafter referred to as "Sun") in view of Shiomoto as applied to claims 1 and 22 above, and further in view of Webb.

The Sun apparatus, now incorporating Shiomoto's differing error resiliency technique for first and second frames, a majority of the features of claims 3-4, as discussed with regards to claim including having the second block comprise a variable length coder (Sun: column 3, lines 40-57), however, the Sun-Shiomoto combination fails to disclose the use of application of resynchronization markers as in the claims. Webb discloses the use of reversible variable length codewords (Webb: column 4, lines 55-68; column 5, lines 1-30) for the application of

resynchronization markers (Webb: column 2, lines 20-35) in order to process video with uncorrectable errors (Webb: column 1, lines 30-65). Accordingly, given this teaching it would have been obvious for one of ordinary skill in the art to incorporate Webb's reversible variable length codewords for the application of resynchronization markers into the Sun-Shiomoto combination in order to have the Sun-Shiomoto combination be able to process video streams with uncorrectable errors. The Sun apparatus, now incorporating Shiomoto's differing error resiliency technique for first and second frames and Webb's use of reversible variable length codewords for the application of resynchronization markers, has all of the features of claims 3-4.

The Sun apparatus, now incorporating Shiomoto's differing error resiliency techniques for first and second frames, has a majority of the features of claim 5, however, the Sun-Shiomoto combination fails to disclose the use of application of resynchronization markers at differing intervals as in the claim. Webb discloses the use of reversible variable length codewords (Webb: column 4, lines 55-68; column 5, lines 1-30) for the application of resynchronization markers (Webb: column 2, lines 20-35) at differing intervals (Webb: column 12, lines 23-55) in order to process video with uncorrectable errors (Webb: column 1, lines 30-65). Accordingly, given this teaching it would have been obvious for one of ordinary skill in the art to incorporate Webb's reversible variable length codewords for the application of resynchronization markers into the Sun-Shiomoto combination in order to have the Sun-Shiomoto combination be able to process video streams with uncorrectable errors. The Sun apparatus, now incorporating Shiomoto's differing error resiliency techniques for first and second frames and Webb's use of reversible variable length codewords for the application of resynchronization markers at differing intervals, has all of the features of claim 5.

The Sun apparatus, now incorporating Shiomoto's differing error resiliency techniques for first and second frames, a majority of the features of claim 9, as discussed with regards to claim including a data partitioning block (Sun: column 3, lines 40-57) and a header extension code block (Sun: column 4, lines 45-67). However, the Sun-Shiomoto combination fails to disclose the use application of a reversible variable length coder block and a resynchronization marker block for application of resynchronization markers as in the claim. Webb discloses the use of reversible variable length codeword block (Webb: column 4, lines 55-68; column 5, lines 1-30) and a resynchronization marker block (Webb: column 2, lines 20-35) in order to process video with uncorrectable errors (Webb: column 1, lines 30-65). Accordingly, given this teaching it would have been obvious for one of ordinary skill in the art to incorporate Webb's reversible variable length codeword block and resynchronization marker block into the Sun-Shiomoto combination in order to have the Sun-Shiomoto combination be able to process video streams with uncorrectable errors. The Sun apparatus, now incorporating Shiomoto's differing error resiliency techniques for first and second frames and Webb's use of reversible variable length codeword block and a resynchronization marker block, has all of the features of claim 9.

The Sun method, now incorporating Shiomoto's differing error resiliency techniques for first and second frames, has a majority of the features of claim 24, however, the Sun-Shiomoto combination fails to disclose the use of application of resynchronization markers at differing intervals as in the claim. Webb discloses the use of reversible variable length codewords (Webb: column 4, lines 55-68; column 5, lines 1-30) for the application of resynchronization markers (Webb: column 2, lines 20-35) at differing intervals (Webb: column 12, lines 23-55) in order to process video with uncorrectable errors (Webb: column 1, lines 30-65). Accordingly, given this

teaching it would have been obvious for one of ordinary skill in the art to incorporate Webb's reversible variable length codewords for the application of resynchronization markers into the Sun-Shiomoto combination in order to have the Sun-Shiomoto combination be able to process video streams with uncorrectable errors. The Sun method, now incorporating Shiomoto's differing error resiliency technique for first and second frames and Webb's use of reversible variable length codewords for the application of resynchronization markers at differing intervals, has all of the features of claim 24.

10. Claims 10-18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sun et al., (hereinafter referred to as "Sun") in view of Shiomoto and Webb.

Sun discloses a processor containing instructions that enable the processor to comprising: receive a video stream having at least a first type of frame (Sun: column 7, lines 50-65; column 9, lines 45-56) and a second type of frame (Sun: column 10, lines 5-10 & 40-67), as in claim 10. However, Sun fails to disclose processing using first and second error resiliency techniques on said first and second respective frame types, wherein the first technique discloses the further use of resynchronization markers at a first interval and the second technique using a differing interval than the first. Shiomoto discloses an error concealment apparatus with differing error resiliency techniques based differing code strings (Shiomoto: column 4, lines 10-60) wherein the second error resilience technique replaces a bit pattern from the second type of frame with a shorter bit pattern (Shiomoto: column 4, lines 30-45) in order to reinforce error-correcting abilities (Shiomoto: column 2, lines 1-6). Accordingly, given this teaching, it would have been obvious for one of ordinary skill in the art to incorporate Shiomoto's differing error concealment techniques for improved error resiliency into the Sun apparatus in order to reinforce error-

correcting abilities. The Sun apparatus, now incorporating Shiomoto's differing error resiliency techniques for the first and second frames, has a majority all of the features of claim 10, however, the Sun-Shiomoto combination fails to disclose the use of application of resynchronization markers as in the claim. Webb discloses the use of reversible variable length codewords (Webb: column 4, lines 55-68; column 5, lines 1-30) for the application of resynchronization markers (Webb: column 2, lines 20-35) in order to process video with uncorrectable errors (Webb: column 1, lines 30-65). Accordingly, given this teaching it would have been obvious for one of ordinary skill in the art to incorporate Webb's reversible variable length codewords for the application of resynchronization markers into the Sun-Shiomoto combination in order to have the Sun-Shiomoto combination be able to process video streams with uncorrectable errors. The Sun processor, now incorporating Shiomoto's differing error resiliency techniques for the first and second frames as executed in software (Webb: column 12, lines 10-20) and Webb's use of reversible variable length codewords for the application of resynchronization markers, has all of the features of claim 10.

Regarding claim 11, the Sun processor, now incorporating Shiomoto's differing error resiliency techniques for the first and second frames as executed in software (Webb: column 12, lines 10-20) and Webb's use of reversible variable length codewords for the application of resynchronization markers, has the first error resilience technique to process a P frame (Shiomoto: column 8, lines 65-67; column 9, lines 1-10).

Regarding claims 12-13, the Sun processor, now incorporating Shiomoto's differing error resiliency techniques for the first and second frames as executed in software (Webb: column 12, lines 10-20) and Webb's use of reversible variable length codewords for the application of

resynchronization markers, has the second error resilience technique to process a B frame (Shiomoto: column 8, lines 65-67; column 9, lines 1-10), as in the claims.

Regarding claim 14, the Sun processor, now incorporating Shiomoto's differing error resiliency techniques for the first and second frames as executed in software (Webb: column 12, lines 10-20) and Webb's use of reversible variable length codewords for the application of resynchronization markers, has inserting the resynchronization markers at differing intervals (Webb: column 12, lines 23-55), as in the claims.

Regarding claim 15, the Sun processor, now incorporating Shiomoto's differing error resiliency techniques for the first and second frames as executed in software (Webb: column 12, lines 10-20) and Webb's use of reversible variable length codewords for the application of resynchronization markers, has the first error concealment technique is different from the second error concealment technique (Sun: column 12, lines 1-40), as in the claim.

Regarding claim 16, the Sun processor, now incorporating Shiomoto's differing error resiliency techniques for the first and second frames as executed in software (Webb: column 12, lines 10-20) and Webb's use of reversible variable length codewords for the application of resynchronization markers, has inserting fewer error resilience bits into the video stream for the B-type frame than for the P-type frame (Shiomoto: column 8, lines 65-67; column 9, lines 1-10), as in the claim.

Regarding claim 17, the Sun processor, now incorporating Shiomoto's differing error resiliency techniques for the first and second frames as executed in software (Webb: column 12, lines 10-20) and Webb's use of reversible variable length codewords for the application of

resynchronization markers, has variable length encoding (Sun: column 7, lines 15-30), as in the claim.

Regarding claim 18, the Sun processor, now incorporating Shiomoto's differing error resiliency techniques for the first and second frames as executed in software (Webb: column 12, lines 10-20) and Webb's use of reversible variable length codewords for the application of resynchronization markers, has applying resynchronization markers to the video for B frames (Webb: column 12, lines 25-60), as in the claim.

Conclusion

11. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

12. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Andy S. Rao whose telephone number is (703)-305-4813. The examiner can normally be reached on Monday-Friday 8 hours.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chris S. Kelley can be reached on (703)-305-4856. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Andy S. Rao
Primary Examiner
Art Unit 2613

ANDY RAO
PRIMARY EXAMINER

asr
August 5, 2004